Mobile Power Guidelines ’99

Intel Corporation

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1. Executive Summary

The demand for new features and higher performance in mobile PCs presents a major challenge to the mobile PC industry in the area of platform power. Power dissipated in the interior of a full-featured notebook has increased by 90% in the last three years. Looking ahead to expected system enhancements, this power consumption could increase to more than 35 watts by 1999. This would create a thermal problem since 1999 notebook computers are only expected to be able to dissipate about the same 23 to 25 watts as today's systems.

Intel's Mobile Power Initiative is a coordinated industry program that addresses these power challenges. It is a comprehensive program that spans across all areas that impact power: platform, operating system, and applications. To address application power, Intel has created power monitoring and analysis tools that help software developers identify and correct power wasting code. To improve operating system power management, Intel, Microsoft and Toshiba authored an industry power management specification called the Advanced Configuration and Power Interface (ACPI.) This Mobile Power Guidelines focuses on the platform power issues by providing achievable power targets for all system components. Meeting these component power targets ensures that mobile PC systems in 1999 will contain all the features and performance that users demand, while holding power to within the thermal limits of today's mobile PCs. Hardware component vendors and original equipment manufacturers will benefit by cost reductions due to lower power components, lighter weight thermal solutions, and higher product reliability.

This document also discusses various techniques that can be used to hit the power targets. Among them, voltage reduction is the most significant method of reducing power. Table 1.1 shows the key component voltage and power changes targeted for systems shipping in mid 1999.

Table 1.1 1999 Key Component Voltage and Power Targets

Component	1998 Estimate		1999 Targets	
	Voltage (Volts)	3D WinBench Power (Watts)	Voltage (Volts)	3D WinBench Power (Watts)
CPU Core	1.6	7.9	1.6 or lower	7.9
Memory Controller	3.3	1.7	1.8	1.2
System Memory	3.3 (SDRAM)	1.7	2.5 (RDRAM®*)	1.4
System Memory Bus	3.3		1.8	
Graphics Controller	3.3	2.0	1.8	2.4
Graphics Frame Buffer	3.3	0.6	Frame Buffer Integrated into Graphics Controller	
Advanced Graphics Port Bus (AGP)	3.3		1.5	
Power Supply	88% Efficient		90% Efficient	

Implementing these voltage and power reduction targets allows the performance improvements customers demand while keeping the overall system power within the 23 to 25 watt thermal envelope. Intel is committed to continuing the voltage reduction trend on mobile system components it manufactures. We encourage mobile computer component and original equipment manufacturers to join this trend. Those who embrace it will reap many benefits including the following:

- ✯ Lower power components
  - ✔ Lower cost component packages
  - ✔ More reliable components
  - ✔ Higher performance
- ✯ Lower power systems
  - ✔ Lower cost thermal solutions
  - ✔ Lighter weight thermal solutions
  - ✔ More reliable systems
  - ✔ More room for additional features or performance

We call upon industry leaders like yourself to join us in bringing about the changes needed to unlock the opportunities on the mobile horizon. Designing your components and systems to meet the Intel Mobile Power Guidelines will benefit both your customers and the mobile PC industry.

2. Introduction

New technologies and feature rich applications are promising unprecedented opportunities for mobile computer system, hardware component, and software vendors. Users expect the same high performance from their mobile computers that they enjoy on their desktops. At the same time mobile computer system design is becoming more challenging.

As we look to the future, we see these opportunities bounded by the thermal realities of mobile computer system design. New systems cannot increase performance or add new features if they can not dissipate the heat. To address this issue, new systems can either find ways to dissipate more heat or find ways to reduce power consumption. In the next few years, we feel there are significant opportunities and benefits in reducing power consumption.

To support this strategy Intel is significantly reducing voltages on mobile system components it manufactures such as microprocessors and chip sets. However, enabling higher performance systems with new features will require lowering the voltage of many other system components to keep the overall system thermally manageable. This will require an industry wide effort to lower bus interface voltages and establish power guidelines. To facilitate this cooperative industry effort, Intel is proposing these "Mobile Power Guidelines."

2.1 Objective

The objective of this document is to unify the mobile computing industry with a common set of guidelines to enable continued feature and performance enhancements in a thermally manageable system.

This document describes the challenges mobile system designers will face in the next few years if nothing is done to manage system power consumption and sets bus interface and component voltage and power targets for 1999 systems. This document describes high-end, full-size, full-featured mobile platforms expected to be in production in mid 1999.

3. Notebook System Power Trends

Notebook computers are becoming increasingly more sophisticated incorporating many of the features of high performance desktop systems. These include such features as high performance processors, second level cache, better graphics, DVD drives, and new I/O busses like USB. As new notebook computer generations are introduced the power required to implement these new features keeps increasing. Projecting this trend forward over the next few years to include features such as larger LCD screens, accelerated 3D graphics, more system memory, and 1394 based I/O devices shows system power requirements increasing significantly.

Table 3.1 shows the growth in full featured notebook interior power since 1994 and projects notebook interior power through 1999 if nothing is done to manage power consumption. Notebook interior power includes all components inside the notebook main chassis. It excludes power for the LCD panel and external connections such as USB and 1394 since they do not add to the thermal energy dissipated in the main notebook chassis.

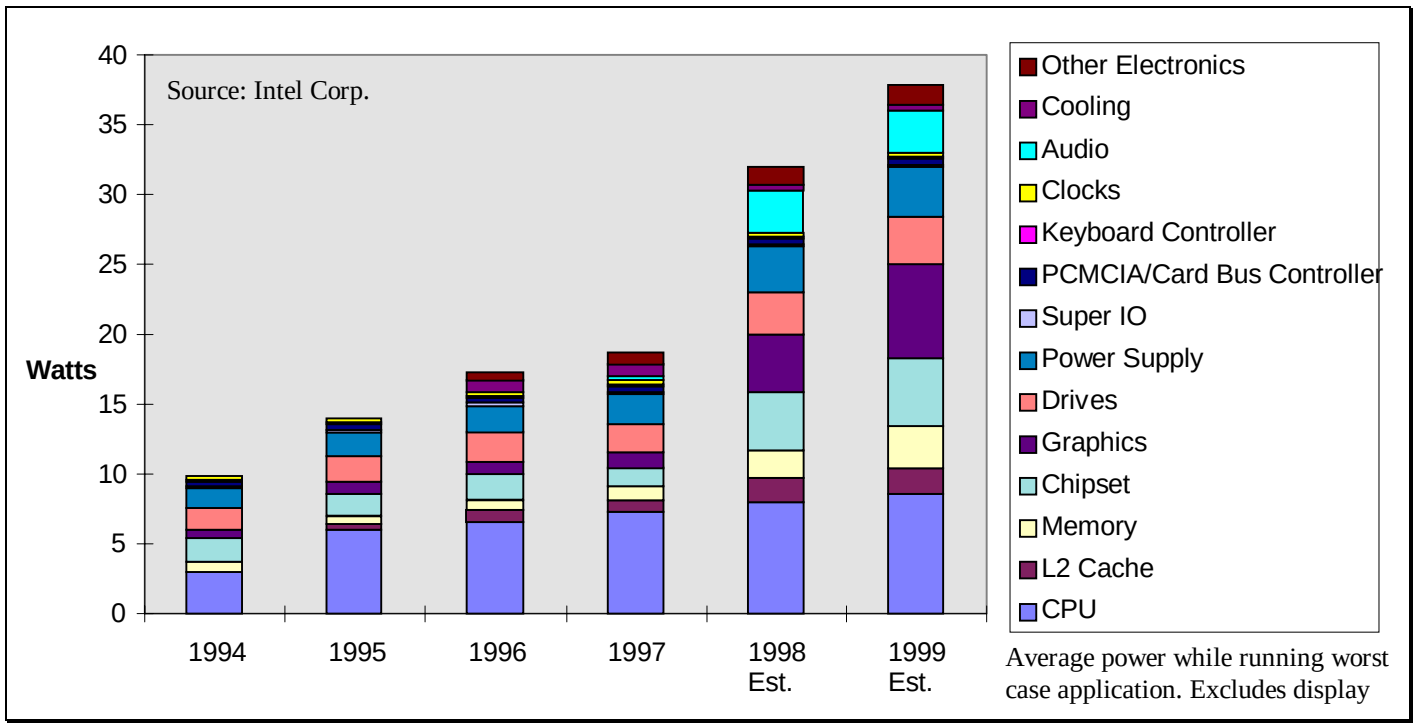

Table 3.1 Unmanaged Notebook Power Trends

This trend shows power dissipated in the notebook interior increasing by 90% between 1994 and 1997 and projects power increasing by another 85% between 1997 and 1999. (See appendix B for power trend data and assumptions.) If this trend in notebook power consumption goes unmanaged, it will soon outpace notebook thermal capabilities limiting future system features and performance.

3.1 Notebook Cooling Capabilities

While notebook power consumption has been increasing rapidly, cooling techniques to remove the heat generated within the notebook have been evolving more slowly. Current notebook systems measuring 8 ½ x 11 inches with base units (excluding lid thickness) between 0.75 inches and 1.5 inches can dissipate about 23 to 25 Watts.[1] This thermal envelope makes the following assumptions:

- Ambient room temperature is approximately 25 °C.
- The bottom surface of the notebook is insulated and the keyboard surface is used as a radiator.
- The notebook skin is made of ABS/PC plastic and has an isothermal skin temperature.
- The notebook uses a combined heat spreader plate, heat pipe, remote heat exchanger, and fan cooling method.

The heat from inside a notebook is dissipated by warming the outside surface (skin) of the plastic over the ambient air and by using a fan and heat exchanger. Most fan designs can remove about 4 to 6 Watts of heat and the rest is passively dissipated by natural

[1] Refer to Intel Application Note 584 "Notebook Thermal Design Guide for High-Powered Microprocessors" (order # 243321-001) for a detailed discussion of notebook thermal considerations.

convection and radiation from the outside surface. If there are no limits on the outside surface temperature, the passive heat dissipation limit is unbounded. Of course, such a notebook with unconstrained high skin temperatures will be unusable. Due to ergonomic constraints limiting notebook computer skin temperature to approximately 15 °C over ambient air temperature, systems in 1999 are likely to still be constrained within the same thermal envelope as today.

Table 3.2 shows the change in skin temperature for a given notebook size, ambient temperature and total power dissipated in the base of the notebook. The dotted lines show the approximate power dissipation limits for an 8.5 x 11 size notebook with a base height between 0.75 inches to 1.5 inches. The total heat dissipation power in the figure does not include the display power. This thermal constraint shows the projected system power is unmanageable and requires action to reduce future notebook system power.

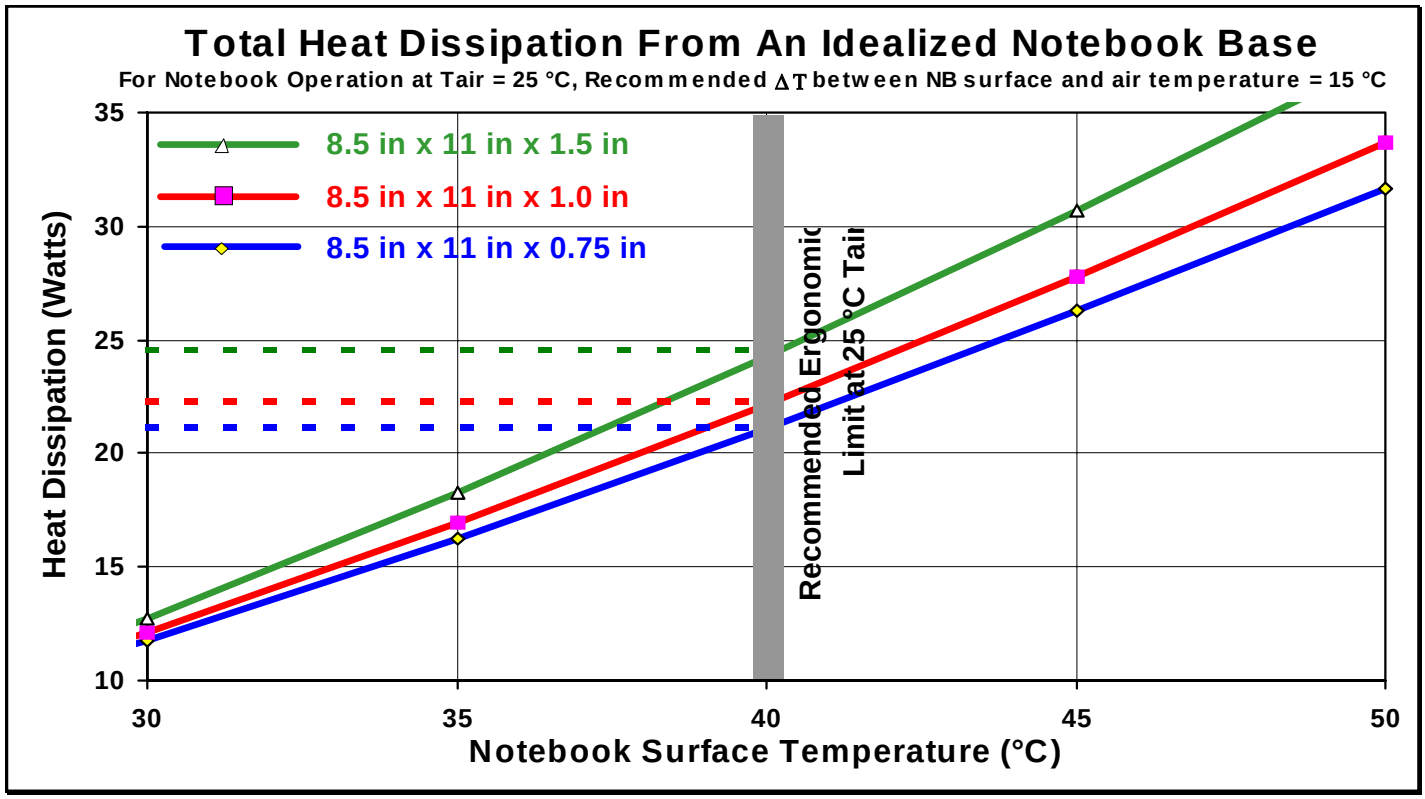

Table 3.2 Heat Dissipation Limits From a Notebook Base

3.1.1 Notebook System Power Targets

To reduce notebook system power to thermally manageable levels we are proposing power targets for each subsystem. Implementing these subsystem power targets will bring the overall notebook power back within the 23 to 25 watt thermal limit. Table 3.3 shows the notebook power targets achievable with industry coordination and illustrates how much power can be saved over the unmanaged system power projections. Subsystem power targets are described in detail in section 5.

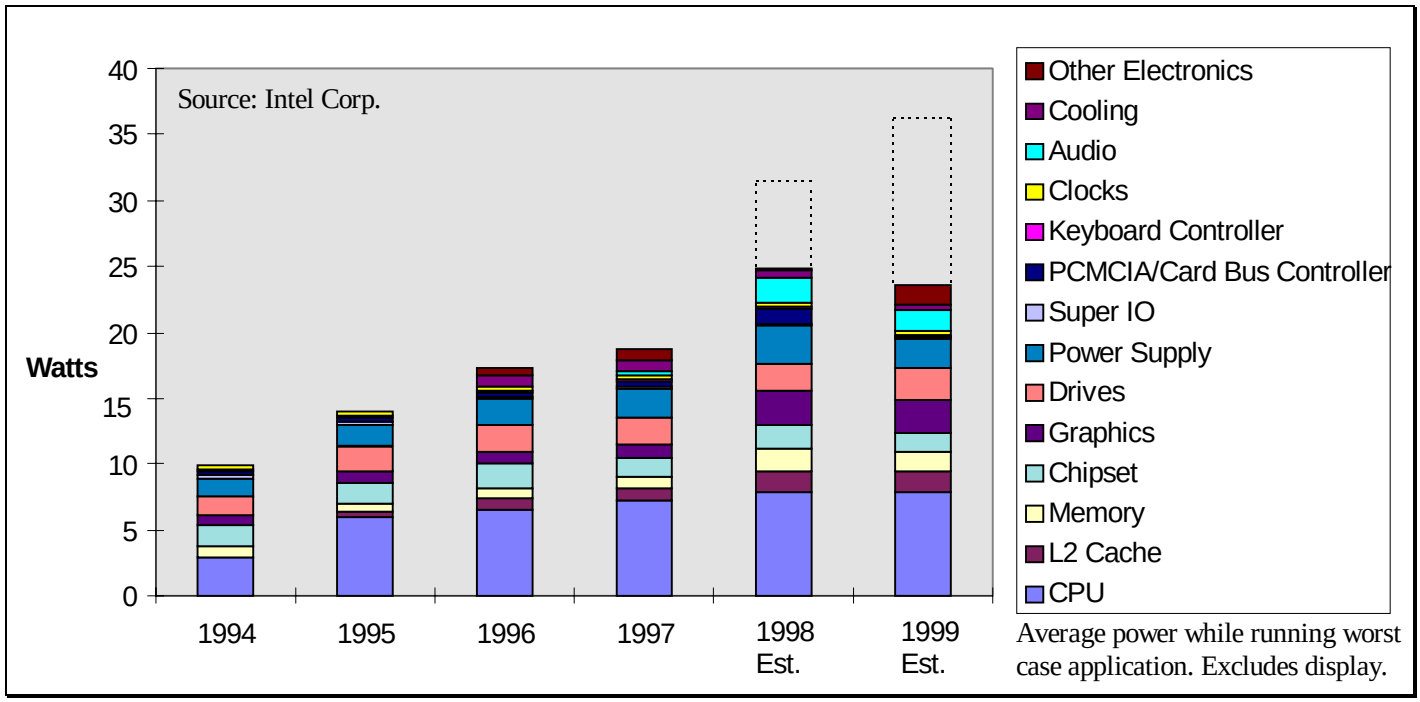

Table 3.3 Notebook Power Targets with Industry Coordination

4. Power Reduction Methods

Meeting the power targets and improving notebook system performance can be accomplished through voltage reduction, component optimization, improvements in device power management and software optimization.

4.1 Voltage Reduction

Power consumed in CMOS circuits is proportional to frequency and voltage as shown in the following equation:

$$\textbf{Power} \propto \textbf{(Capacitance * Frequency * (Voltage)}^2\textbf{) + (Voltage * (DC Current + Leakage Current))}$$

The DC and leakage currents tend to be small for CMOS circuits which makes the CFV^2 term dominate this equation. Reducing the frequency reduces power linearly. However, it has the disadvantage of reducing performance linearly as well. Reducing the voltage has the advantage of reducing power as the square of the voltage. Furthermore, components optimized for lower voltage operation also benefit from improved performance since they can operate at higher speeds. Therefore, voltage reduction yields the biggest component power improvement.

Intel is improving system performance and holding down power consumption by significantly reducing voltages on microprocessors and chipsets. Additionally, Intel is actively promoting low voltage interfaces such as 1.8 volt cache and direct RDRAM™* signaling, and 1.5 volt Advanced Graphics Port (AGP) signaling. To add new features and increase performance in other parts of the system, more system components need to move to lower voltages.

4.1.1 Component Core Voltages

Table 4.1 shows Intel's proposed mobile component core voltage targets through the year 1999.

Table 4.1 Proposed Mobile System Component Core Voltages

	1997	1998	1999
CPU Core	1.8 V	1.6 V	1.6 V or lower
L2 Cache	3.3 V	3.3 V	3.3 V
Memory Controller	3.3 V	3.3 V	1.8 V
System Memory	3.3 V (EDO / SDRAM)	3.3 V (EDO / SDRAM)	2.5 V (RDRAM)
Graphics controller	3.3 V	2.5 V	1.8 V
Graphics Frame Buffer	3.3 V (EDO / SDRAM)	3.3 V (EDO / SDRAM / RDRAM)	3.3 V or Integrated
I/O Controller	3.3 V	3.3 V	2.5 V
LCD Logic	5 V	5 V or 3.3 V	3.3 V
Backlight inverter	Battery voltage	Battery voltage	Battery voltage
FLASH EPROM	3.3 V	3.3 V	3.3 V
Audio (Digital)	3.3 V	3.3 V	2.5 V
Audio CODEC	5 V	5 V	3.3 V
Super I/O	3.3 V	3.3 V	2.5 V
1394 Controller	None	None	3.3 V
CardBus Controller	3.3 V	3.3 V	2.5 V
LAN	3.3 V (PC Card or dock)	3.3 V (PC Card or dock)	3.3 V
MODEM DSP	3.3 V	3.3 V	Soft Modem
MODEM CODEC / DAA	5 V	5 V	3.3 V

4.1.2 Bus Signaling Voltages

Table 4.2 shows Intel's proposed bus voltage targets through the year 1999.

Table 4.2 - Proposed Bus Interface Voltages

	1997	1998	1999
CPU Host Bus	2.5 V (CMOS)	1.6 V (GTL)	1.6 V or lower (GTL)
CPU Cache Bus	NONE	1.8 V	1.8 V
Memory Bus	3.3 V (EDO / SDRAM)	3.3 V (EDO / SDRAM)	1.8 V (Direct RDRAM)
Graphics Interface	3.3 V (PCI)	3.3 V (AGP)	1.5 V (AGP)
Graphics Frame Buffer Bus	3.3 V (EDO / SDRAM)	3.3 V (EDO / SDRAM / RDRAM or integrated)	integrated (or EDO / SDRAM / RDRAM)
LCD Interface	5 V	0.7 V (LVDS or panel link)	0.7 V (LVDS or panel link)
PCI Bus	3.3 V	3.3 V	3.3 V
ISA subset Bus	3.3 V	3.3 V	NONE
IDE	3.3 V / 5 V safe	3.3 V / 5 V safe	3.3 V / 5 V safe
Floppy Drive Interface	3.3 V / 5 V safe	3.3 V / 5 V safe	3.3 V / 5 V safe
USB Signaling	3.3 V	3.3 V	3.3 V
CardBus	3.3 V	3.3 V	3.3 V
1394 Link Interface	NONE	NONE	2.5 V
1394 Physical Interface	NONE	NONE	3.3 V
SMBUS	3.3 V	3.3 V	3.3 V
Parallel Port	3.3 V (5 V safe)	3.3 V (5 V safe)	3.3 V (5 V safe)
Serial Port	+/-12 V RS232	+/-12 V RS232	+/-12 V RS232

4.2 Component Optimization

In addition to reducing component voltages, integrated circuits can be made more power efficient through design optimization. During integrated circuit design, benchmarks can be developed to identify where power is being consumed on a unit by unit basis. Once the power distribution profile is characterized, low power design techniques such as gating the clock to unused sections of circuitry or reducing the number of nodes toggling for a given operation can be implemented. Buffer design can also be optimized to reduce power by not overdriving signals. Implementing these design optimization techniques can significantly reduce both idle and active power.

4.3 Device Power Management

Intel, Microsoft, and Toshiba defined a power management interface called the Advanced Configuration and Power Interface (ACPI). ACPI defines system and device power states and a consistent register interface for device configuration and control. This allows better component power management allowing components to spend more time in low power states. This will help reduce the system thermal load and will improve battery life for typical applications. The amount of power saved will be influenced significantly by application and usage patterns. Refer to Appendix C for a brief description of the defined ACPI system and device power states.

4.4 Software Optimization

Software can be optimized to conserve power by eliminating loops and software sequences that prevent the system from going into low power idle states and by optimizing software design. Intel has developed guidelines and tools to assist software developers in making their programs more power friendly. This includes a software tool called the Intel Power Monitor (IPM). This tool monitors and displays system activity allowing software vendors to identify programs that are wasting power. If the power monitor detects specific power wasting code loops, it can demonstrate the impact of fixing the software by temporarily updating the running code to be more power friendly. The Intel power monitor is available on the world wide web at http://www.intel.com/ial/ipm.

5. System Feature and Power Targets

This section describes system feature assumptions and power targets for 1999 notebook computers. 1998 feature and power figures are included for comparison. Section 5.1 shows the system configuration assumptions. Section 5.2 proposes power targets for each subsystem and summarizes the total power dissipated in the notebook interior. Section 5.3 provides more detail on the subsystem power targets and shows utilization assumptions. It also provides implementation ideas and design considerations.

5.1 System Configurations

Table 5.1 shows the system configuration assumptions for mid 1998 and mid 1999 systems. This only describes high-end, full-featured systems implementing the latest technology since these will be the systems pushing the thermal envelope. It is assumed that solving the thermal problem for high-end systems will automatically solve it for full-sized mid-range and entry level systems.

Table 5.1 - 1998 and 1999 System Configuration Assumptions

1998 System Configuration	1999 System Configuration
• Mobile Pentium® II processor	• Mobile Pentium® II processor or next generation
• 512 KB pipeline burst level two cache	• 512 KB pipeline burst level two cache
• Graphics controller AGP 1x interface 4 MB frame buffer 1024 x 768 x 18 bit / pixel resolution MPEG2 H/W assist (motion compensation, YUV 4:2:0) 3D acceleration LCD and CRT dual screen support LVDS or Panel Link display interface	• Graphics controller AGP 2x interface 4 MB frame buffer 1024 x 768 x 24 bit / pixel resolution MPEG2 H/W assist (motion compensation, YUV 4:2:0) Enhanced 3D acceleration LCD and CRT dual screen support LVDS or Panel Link display interface TV output
• 13.3” Color TFT LCD display	• 13.3” Color TFT LCD display
• Memory Subsystem 32MB EDO or SDRAM memory	• Memory Subsystem 64MB RDRAM memory
• I/O Subsystem I/O controller with integrated timers, counters, etc. 3.3v 33 MHz PCI bus Fast IR System Management Bus controller Universal Serial Bus controller Parallel and serial ports Keyboard controller ACPI microcontroller with SM Bus system battery interface 3.3 / 5v ISA subset bus	• I/O Subsystem I/O controller with integrated timers, counters, etc. 3.3v 33 MHz PCI bus Fast IR System Management Bus controller Universal Serial Bus controller Parallel and serial ports Keyboard controller ACPI microcontroller with SM Bus system battery interface
	• 1 1394 walk-up port (S400)
• 1 USB port	• 1 USB port
• Storage media Floppy drive IDE hard drive IDE DVD-ROM	• Storage media Floppy drive IDE hard drive IDE DVD-ROM in swap bay
• CardBus 2 slots	• CardBus 2 power managed slots
• Audio Sound blaster H/W compatible Wavetable synthesis (down loadable samples) 3D positional sound AC3 / MPEG2 decode Full duplex G.723.1 encode/decode with acoustic echo cancel. Host controller	• Audio Sound blaster S/W emulation Wavetable synthesis (down loadable samples) 3D positional sound AC3 / MPEG2 decode Full duplex G.723.1 encode/decode with acoustic echo cancel. Host controller
• Data, fax, voice modem including V.80 support	• Software modem data pump
• PCI Docking	• PCI Docking
• LAN on CardBus card	• LAN on motherboard

5.2 System Power Targets

This section proposes power targets for each subsystem and summarizes the total power dissipated in the notebook interior.

To define system power targets it is necessary to identify the applications that generate the worst case system thermal power that is likely to occur in normal use. Appendix A shows system power measurements for several applications measured on an Intel evaluation board in 1997. These tests identified MPEG2 video playback as having the worst case thermal power of the applications we tested. Extrapolating this data and factoring in significant system improvements such as multimedia enhancements, we expect the worst case power applications in 1998 and 1999 to be MPEG2 video playback and 3D game play. While these applications are not expected to be the most commonly used applications they are expected to be the worst case power applications since they both are CPU intensive requiring a lot of video and audio decompression, high resolution, fast action graphics, DVD drive and memory accesses, and audio playback.

The 3D game scenario assumes scenes are stored on an IDE DVD drive, the hard drive is accessed occasionally, and audio is active at 30% amplifier power. A CardBus LAN card is connected in the 1998 scenario and in 1999 an onboard LAN is connected. The LAN is assumed to be predominantly idle. In 1999 the CardBus slots are assumed empty.

The MPEG2 movie scenario assumes the movie is playing from an IDE DVD drive, hard drive is powered off, and audio is active at 30% amplifier power. The CardBus slots are unused. In 1999 the onboard LAN is assumed connected but mostly idle.

In this document power is specified in terms of peak power, idle power, and average power while running the 3D game and MPEG2 applications. Since it is difficult to benchmark power consumption during 3D game play, the power targets for most subsystems are specified while running the benchmark program 3D WinBench*. 3D WinBench power is assumed to be similar to 3D game power consumption.

Peak power refers to the highest power a subsystem will draw at nominal Vcc and maximum performance (i.e. CPU doing floating point calculations at top frequency with most data hitting the level 1 cache, DRAM reading at peak bandwidth, etc.) This peak performance assumes the subsystem is utilized at 100% capacity and that it draws maximum power at maximum performance. Idle power refers to the power a subsystem will draw at nominal Vcc when it is not processing data. This is defined as 0% utilization. During normal system operation most subsystems are utilized at some percentage of their maximum capacity and maximum power. This document assumes that for most subsystems power consumption scales linearly with utilization between idle power and peak power. This is illustrated in Table 5.2. For some components, such as an audio accelerator, power does not scale linearly with utilization. For these components, power was estimated individually and summed with the rest of the subsystem. For components where power is approximately linear with utilization, the average thermal power for a subsystem running a particular application can be estimated with the following equation:

Subsystem Average Thermal Power = (Subsystem Peak Power * Utilization) + (Subsystem Idle Power * (1 - Utilization))

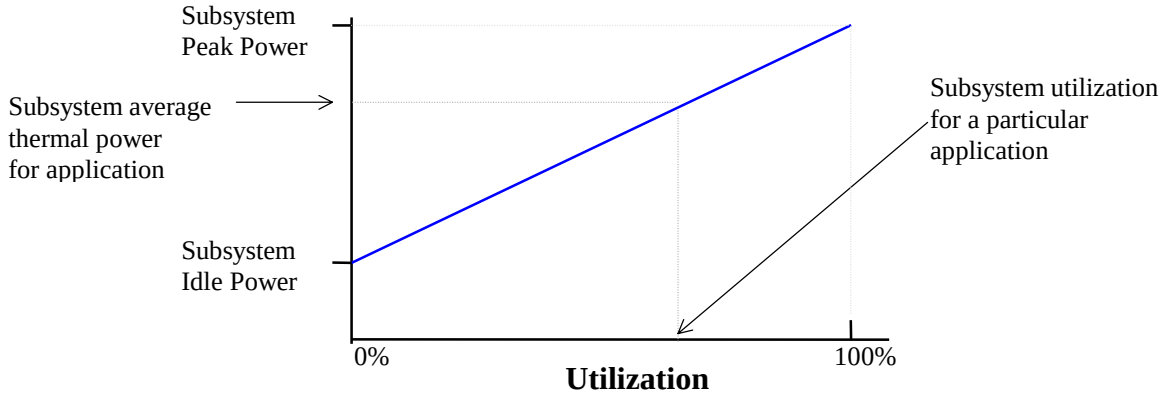

Table 5.2 Subsystem Average Thermal Power

The worst case system thermal power is the sum of the average thermal power for each subsystem while running the worst case power application. Table 5.3 shows a summary of the proposed 1999 power targets for the 3D game and MPEG 2 movie scenarios. 1998 power targets are included for comparison.

Table 5.3 System Power Target Summary (Notebook interior. Excludes Display)

	Estimated 1998 Power (Watts)		1999 Power Goals (Watts)	
	3D Game	MPEG 2 Movie	3D Game	MPEG 2 Movie
CPU core	7.9	6.5	7.9	6.5
L2 Cache	1.6	1.4	1.6	1.4
Memory Controller	1.7	1.7	1.2	0.9
System Memory	1.7	1.7	1.4	1.4
Graphics Subsystem	2.6	2.6	2.4	2.4
IO Subsystem	0.5	0.7	0.5	0.6
Audio	2.0	2.0	1.5	1.5
Hard Drive	0.7	0.0	0.7	0.0
DVD Drive	1.4	3.0	1.4	3.0
1394 Controller	0.0	0.0	0.0	0.0
USB	0.0	0.0	0.0	0.0
CardBus	1.2	0.2	0.1	0.1
LAN	0.0	0.0	0.4	0.4
Power Supply	2.8	2.7	2.0	2.0
Charging	0.1	1.0	0.1	1.0
Cooling	0.5	0.5	0.5	0.5
Other	0.5	0.5	0.3	0.3
Total	**25.2**	**24.5**	**22.0**	**22.0**

5.3 Subsystem Power Targets

The following sections elaborate on the power targets, utilization assumptions, and implementation suggestions for each subsystem. Subsystem utilization projections are based on measured subsystem power and adjusted for estimated changes due to higher bit rate data streams, higher bandwidth busses (AGP, RDRAM, etc.), and higher performance subsystems.

5.3.1 CPU and Level Two Cache

5.3.1.1 Features

The following CPU and level two cache subsystem features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• Mobile Pentium® II Processor • 512 KByte level two cache	• Mobile Pentium® II Processor or next generation • 512 KByte level two cache

5.3.1.2 Power Targets

The following table shows the CPU and Level two cache power targets and utilization assumptions for 1998 and 1999.

	Estimated 1998 CPU & L2 Cache Power				1999 CPU & L2 Cache Power Targets			
	Peak Power (W)	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**	**Peak Power (W)**	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**
CPU	9.5	0.4	7.9	6.5	9.5	0.4	7.9	6.5
L2	2.8	0.6	1.6	1.4	2.8	0.6	1.6	1.4
CPU Utilization			80%	65%			80%	65%
L2 Utilization (tag / data)			24%/50%	19%/40%			24%/50%	19%/40%

Average 3D WinBench power represents the highest *sustained* power that a real worst-case application will draw from the CPU. The typical thermal design power (TDP typical) specification for an Intel processor is derived from sustained power measurements from worst case applications such as 3D WinBench with margin added to account for process variations. The peak CPU power guideline represents the maximum power consumed while executing the worst case CPU instruction mix at nominal Vcc. This resembles the TDP max specification for Intel processors. These are design guidelines and should not be construed as future processor specifications.

The CPU average power includes 15% CPU to memory controller bus utilization (0.2 Watts). CPU core thermal design power is held at or below 8 watts through 1999.

5.3.2 Memory Controller

5.3.2.1 Features

The following memory controller features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• EDO/SDRAM interface • AGP 1x graphics interface • 1.6v CPU interface	• Direct RDRAM interface • AGP 2x graphics interface • 1.6v or lower CPU interface

5.3.2.2 Power Targets

The following table shows the memory controller power estimates and utilization assumptions for 1998 and targets for 1999.

Estimated 1998 Memory Controller Power				1999 Memory Controller Power Targets			
Peak Power (W)	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**	**Peak Power (W)**	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**
2.6	0.4	1.7	1.7	1.6	0.3	1.2	0.9
Utilization		67%	67%			67%	50%

Memory controller power can be reduced by reducing the core voltage from 3.3v in 1998 to 1.8v in 1999.

5.3.3 System Memory

5.3.3.1 Features

The following system memory features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• 32 Mbytes SDRAM	• 64 Mbytes Direct RDRAM

5.3.3.2 Power Targets

The following table shows system memory power estimates and utilization assumptions for 1998 and targets for 1999.

Estimated 1998 Memory Power				1999 Memory Power Target			
Peak Power (W)	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**	**Peak Power (W)**	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**
2.2	0.35	1.7	1.7	2.4	0.35	1.4	1.4
Utilization		72%	72%			50%	50%

The 1999 RDRAM scenario assumes a memory configuration with eight 64 Mbit RDRAM chips. When inactive all chips are assumed to be in the nap state. When active, one chip is assumed active, one chip in standby, and the rest are in the nap state.

Memory performance can be significantly increased without increasing memory power by moving to 2.5v RDRAM instead of 3.3 volt SDRAM.

5.3.4 Graphics

5.3.4.1 Features

The following graphic subsystem features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• AGP 1x interface • 4 MB frame buffer • 1024 x 768 x 18 bit / pixel resolution • Motion Compensation • 3D acceleration • YUV 4:2:0 • LCD and CRT dual screen support • LVDS or Panel Link display interface	• AGP 2x interface • 4 MB frame buffer • 1024 x 768 x 24 bit / pixel resolution • Motion Compensation • Enhanced 3D acceleration • YUV 4:2:0 • LCD and CRT dual screen support • LVDS or Panel Link display interface • TV output

5.3.4.2 Performance Targets

The following table shows graphics subsystem performance targets for 1998 and 1999. The MPEG 2 frame rate performance assumes 720 x 480 pixel main level, main profile video with software decompression / decryption. It also assumes a 10 Mbyte / second video stream.

Estimated 1998 Graphics Performance		1999 Graphics Performance Targets	
3D WinBench Score	**MPEG 2 Frame Rate (fps)**	**3D WinBench Score**	**MPEG 2 Frame Rate (fps)**
85+	30	100+	30

5.3.4.3 Power Targets

The following table shows estimated graphics subsystem power and utilization for 1998 and targets for 1999.

Estimated 1998 Graphics Power				1999 Graphics Power Targets			
Peak Power (W)	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**	**Peak Power (W)**	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**
3.1	1.4	2.6	2.6	3.0	0.8	2.4	2.4
Graphic Ctrl. Utilization		75%	75%			75%	75%
Frame Buff. Utilization		60%	60%			60%	60%

The graphics subsystem performance can be increased in 1999 and meet the 1999 power targets through the following power reduction techniques:

- Reduce the graphic controller core voltage to 1.8 volts.
- Integrate the frame buffer.
- Gate the clock to unused sections of circuitry
- Dynamically change the 3D acceleration clock to allow high performance when needed and low power when the system reaches a thermal limit or low battery constraint.

5.3.5 Flat Panel Display

5.3.5.1 Features

The following flat panel display features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• 13.3” Color active matrix LCD panel • 1024 x 768 x 18 bit / pixel resolution • LVDS or Panel Link display interface • 80 nits panel brightness	• 13.3” Color active matrix LCD panel • 1024 x 768 x 24 bit / pixel resolution • LVDS or Panel Link display interface • 80 nits panel brightness

5.3.5.2 Power Targets

The following table shows estimated flat panel display power and utilization for 1998 and targets for 1999.

Estimated 1998 Flat Panel Display Power			1999 Flat Panel Display Power Targets		
Peak Power (W)	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**	**Peak Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**
3.3	3.3	3.3	2.3	2.3	2.3
Utilization	100%	100%		100%	100%

These power targets include panel logic, backlight, and low voltage signaling interface. Flat panel display power can be reduced through the following techniques:

- Reduce display logic voltage to 3.3 volts.
- Reduce refresh rate when image is static.
- Improve aperture ratio.
- Increase lamp efficiency.
- Increase light spreader sheet efficiency.
- Use Brightness Enhancing Films (BEF).
- Improve panel driver and controller efficiency.
- Improve CCFT inverter efficiency.

5.3.6 I/O Subsystem

5.3.6.1 Features

The following I/O subsystem features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• 3.3v 33 MHz PCI bus • IDE controller • Timers, DMA, RTC • USB controller • System Management Bus controller • Keyboard controller • Super I/O controller (parallel, serial ports, floppy) • Fast IR • ACPI power management controller with SM Bus interface for system battery • 3.3v / 5v ISA subset bus	• 3.3v 33 MHz PCI bus • IDE controller • Timers, DMA, RTC • USB controller • System Management Bus controller • Keyboard controller • Super I/O controller (parallel, serial ports, floppy) • Fast IR • ACPI power management controller with SM Bus interface for system battery

5.3.6.2 Power Targets

The following table shows estimated I/O subsystem power and utilization for 1998 and targets for 1999.

Estimated 1998 I/O Subsystem Power				1999 I/O Subsystem Power Targets			
Peak Power (W)	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**	**Peak Power (W)**	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**
1.3	0.2	0.5	0.7	0.8	0.4	0.5	0.6
I/O Controller		25%	60%			25%	60%
Keyboard Controller		75%	0%			75%	0%
Super I/O		0%	0%			0%	0%
Fast IR		0%	0%			0%	0%
ACPI MicroCtrl		30%	5%			30%	5%

I/O subsystem power can be reduced by lowering I/O component core voltages to 2.5 volts.

5.3.7 1394

5.3.7.1 Features

The following 1394 features are assumed in 1999 systems.

1999 Features
• 1 S400 walk-up port

5.3.7.2 Power Targets

1999 1394 Controller Power Targets					
Peak Power (W)	**Standby Power (W)**	**Disable Power (W)**	**Suspend Power (W)**	**Average 3D Game Power (W)**	**Average MPEG 2 Power (W)**
1.0	0.9	0.4	0.005	0.005	0.005
Utilization				0%	0%

This table makes the following assumptions:

- The power targets apply to a single physical and link layer (PHY/link) 1394 interface. This assumes the PHY core consumes 0.4 W, link consumes 0.4 W, and each PHY port consumes 0.1 W.
- Peak power is consumed when a node's link is on and the PHY core and all ports are also on.
- In Standby, the PHY and all included ports are assumed to be on, and most of the link is on to support wake-up of a "sleeping" attached device. This configuration allows the device to conserve power, while the node's 1394 interface continues to function as a normal bus relay.
- In the Disabled state, the PHY core is on, the link is off, and all of the PHY ports are either suspended or disabled. .
- In the Suspended state, the node's link is off, the PHY core PLL is off and the PHY is almost completely off, retaining only an ability to receive, generate or propagate wake-up notification over the bus. In that state, individual ports are expected to consume on the order of 2 to 5 milliwatts each.
- The MPEG2 and 3D game scenarios assume that there are no 1394 devices connected and that the 1394 controller is in the suspend state.

1394 devices present special power problems in a mobile system. This is due to the inherently high power consumption of a 1394 interface, as well as to the bus requirement to always keep all bus nodes active as bus repeaters. Intel is aggressively working to add power management features to 1394, under the auspices of the IEEE 1394a Working Group and the 1394 Trade Association Power Management Working Group.

The potential benefits of using 1394 should be carefully weighed against the power consumption cost to mobile systems.

5.3.8 USB Port

5.3.8.1 Features

The following USB features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• 1 USB port	• 1 USB port

5.3.8.2 Power Targets

The following table shows estimated USB power and utilization for 1998 and targets for 1999.

	Estimated 1998 USB Power				1999 USB Power Targets			
	Peak Device Power (W)	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**	**Peak Device Power (W)**	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**
Device	2.5	0	0	0	2.5	0	0	0
Utilization			0%	0%			0%	0%

The 3D and MPEG 2 scenarios assume no USB devices are attached.

5.3.9 Audio

5.3.9.1 Features

The following audio subsystem features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• Sound Blaster* H/W compatible • Wavetable synthesis (Down loadable samples) • 3D positional sound • AC3 / MPEG 2 decode • Full duplex G.723.1 encode/decode with acoustic echo cancellation • Data, fax, voice modem including V.80 support • Host controller	• Sound Blaster S/W emulation • Wavetable synthesis (Down loadable samples) • 3D positional sound • AC3 / MPEG 2 decode • Full duplex G.723.1 encode/decode with acoustic echo cancellation • Software modem data pump and host controller

5.3.9.2 Power Targets

The following table shows estimated audio subsystem power and utilization for 1998 and targets for 1999.

Estimated 1998 Audio Power				1999 Audio Power Targets			
Peak Power (W)	**Idle Power (W)**	**Average 3D Game Pwr (W)**	**Average MPEG 2 Pwr (W)**	**Peak Power (W)**	**Idle Power (W)**	**Average 3D Game Pwr (W)**	**Average MPEG 2 Pwr (W)**
4	0.05	2	2	3	0.05	1.5	1.5
Accelerator & DSP		75%	75%			75%	75%
Analog Codec		90%	90%			90%	90%
Modem Codec		0%	0%			0%	0%
Audio Amplifier		30%	30%			30%	30%
Internal Speakers		30%	30%			30%	30%

These power targets assume 65 db sound pressure level at one meter from the speaker.

Audio subsystem power can be reduced in 1999 through the following methods:

- Reduce digital accelerator from 3.3v to 2.5v
- Reduce analog CODECs from 5v to 3.3v
- Balance audio processing between hardware and software
- Increase amplifier and speaker efficiency

5.3.10 Hard Drive / DVD Drive

5.3.10.1 Features

The following storage media features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• IDE hard drive • IDE DVD-ROM	• IDE hard drive • IDE DVD-ROM in swap bay

5.3.10.2 Power Targets

The following tables show estimated storage media power and utilization for 1998 and targets for 1999.

Estimated 1998 Storage Media Power							
	Spin Up Pwr (W)	**Rd/Wr Power (W)**	**Idle Pwr - Spin (W)**	**Standby - No Spin (W)**	**Sleep Pwr (W)**	**Ave 3D Game Power (W)**	**Ave MPEG Power (W)**
H/D	6	2.7	1	0.3	0.1	0.7	0
DVD	6	3	2	0.3	0.1	1.4	3
Hard Drive Utilization					Spin	2%	Power off
					Rd/Wr	5%	
					Idle - spin	31%	
					Standby - no spin	63%	
DVD Drive Utilization					Spin	4%	0%
					Read	30%	100%
					Idle - spin	6%	0%
					Standby - no spin	60%	0%

1999 Storage Media Power Targets							
	Spin Up Pwr (W)	**Rd/Wr Power (W)**	**Idle Pwr - Spin (W)**	**Standby - No Spin (W)**	**Sleep Pwr (W)**	**Ave 3D Game Power (W)**	**Ave MPEG Power (W)**
H/D	6	2.7	1	0.3	0.1	0.7	0
DVD	6	3	2	0. 3	0.1	1.4	3
Hard Drive Utilization					Spin	2%	Power off
					Rd/Wr	5%	
					Idle - spin	31%	
					Standby - no spin	63%	
DVD Drive Utilization					Spin	4%	0%
					Read	30%	100%
					Idle - spin	6%	0%
					Standby - no spin	60%	0%

5.3.11 CardBus

5.3.11.1 Features

The following CardBus subsystem features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• 2 CardBus slots - LAN card in one slot	• 2 power managed CardBus slots - Both slots empty

5.3.11.2 Power Targets

	Estimated 1998 CardBus Power				1999 CardBus Power Targets			
	Peak Power (W)	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**	**Peak Power (W)**	**Idle Power (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**
Ctrl.	0.35	.2	.2	.2	0.35	0.1	0.1	0.1
Slots	5	1	1	0	5	0	0	0
Controller Utilization			5%	5%			0%	0%
Slot Utilization			5%	0%			0%	0%

The 1998 system configuration assumes a LAN card is connected but predominantly idle.

In 1999 the CardBus controller could reduce active power by moving the core voltage to 2.5 volts. Idle power could be reduced by internally gating the PCI clock when no cards are detected.

Intel and Compaq are currently co-chairing a PCMCIA committee defining CardBus power management. The output from this committee will be reflected in the Mobile Power Guidelines when ratified.

5.3.12 LAN

5.3.12.1 Features

The following LAN subsystem features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• CardBus LAN	• LAN on motherboard

5.3.12.2 Power Targets

1999 LAN Power Targets				
Peak Power (W)	**Idle Power - Connected (W)**	**Idle Power - No Connect (W)**	**Average 3D WinBench Power (W)**	**Average MPEG 2 Power (W)**
0.6	0.4	0	0.4	0.4
Utilization			5%	5%

This assumes a 100 base T LAN solution in 1999. The LAN is assumed predominantly idle with less than 5 Mbit / second traffic.

5.3.13 Power Supply

5.3.13.1 Features

The following power supply features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• 88% overall efficiency at maximum load	• 90% overall efficiency at maximum load

5.3.13.2 Design Considerations

Reducing resistance in the power path can significantly reduce power supply losses. Reducing transistor on-resistance (R_{DSon}), inductor resistance, capacitor effective series resistance (ESR) and eliminating the current sense resistor typically found in buck converters can improve power supply efficiency by several percent at high current loads.

While I^2R resistive losses dominate efficiency at high loads, reducing switching losses is also important. Switching losses can be improved by reducing the high-side MOSFET gate-drain charge and gate-source charge, and synchronous MOSFET gate-drain charge and reverse recovery time. For optimum efficiency, the high side MOSFET should be sized to balance resistive losses and switching losses. The power supply controller can reduce switching losses by reducing the dead time between high-side MOSFET and synchronous MOSFET activation. This may require speeding up transistor turn-on / turn off delays.

Lowering the battery and AC adapter input voltages can also reduce power supply switching losses. Most notebook systems currently use a 10.8v battery with AC adapter inputs as high as 18v to 22v. The AC adapter input needs to be higher than the battery voltage to charge the battery. When battery charging is not required, reducing the AC adapter voltage to 10v to 12v could improve power supply efficiency by 2 to 3%. This assumes the AC adapter is external.

The following table lists suggested power supply characteristics for 1998 and 1999 systems. The current load estimates are based on the configuration discussed in this document. Maximum load efficiency refers to the overall power supply efficiency while running a worst case power application such as a 3D game (22 - 25 watts total system power.)

		1998 Power Supply Characteristics					1999 Power Supply Characteristics				
Input Voltage		3-Cell Li+ Battery 7.5-18 V			or 4-Cell Li+ Battery 10-22 V		3-Cell Li+ Battery 7.5-18 V			or 4-Cell Li+ Battery 10-22 V	
Output Voltage	Value	1.6 V	1.8 V	2.5 V	3.3 V	5.0 V	1.6 V	1.8 V	2.5 V	3.3 V	5.0 V
	Regulation and Ripple	3.5%	2%	2%	2%	2%	3.5%	2%	2%	2%	2%
Current	Typ. Load	3 A	0.3 A	1 A	1.5 A	1 A	3 A	2 A	1 A	1.5 A	0.5 A
	Max. Load	6 A	0.5 A	2 A	3 A	4 A	6.5 A	3 A	2.5 A	2.5 A	2.5 A
Efficiency	Max Load	**88%**					**90%**				
Transient	Regulation	7.5%	5%				7.5%	5%			
	Response Time	2µs	2µs				2µs	2µs			

5.3.14 Battery Charging

5.3.14.1 Features

The following battery charging subsystem features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• Adaptive charging algorithm	• Adaptive charging algorithm

5.3.14.2 Power Targets

Estimated 1998 Battery Charging Power				1999 Battery Charging Power Targets			
Peak Power (W)	**Idle Power (W)**	**Average 3D Game Pwr (W)**	**Average MPEG 2 Pwr (W)**	**Peak Power (W)**	**Idle Power (W)**	**Average 3D Game Pwr (W)**	**Average MPEG 2 Pwr (W)**
	0	0.1	1		0	0.1	1

These charging power targets assume an adaptive charging mechanism is implemented. In this document adaptive charging refers to some form of variable charging control that senses how heavily the system is loaded and reduces heat dissipated in charging when the system is near maximum load. Adaptive charging could be implemented through a small sense resistor on the main AC adapter input and adjust charging current to keep overall system power below a maximum threshold. Since the charging voltage is high, the current would be relatively low and a small sense resistor would only dissipate about 0.1 watts at peak load. Adaptive charging could also be implemented with thermal sensors that reduce charging when the system is nearing it's thermal limit.

5.3.15 Cooling

5.3.15.1 Features

The following cooling features are assumed in 1998 and 1999 systems.

1998 Features	1999 Features
• Remote heat exchanger and fan	• Remote heat exchanger and fan

5.3.15.2 Power Targets

The following table shows estimated cooling power and utilization for 1998 and targets for 1999.

Estimated 1998 Cooling Power				1999 Cooling Power Target			
Fan On (W)	Fan Off (W)	3D Game (W)	MPEG2 (W)	Fan On (W)	Fan Off (W)	3D Game (W)	MPEG2 (W)
0.5	0	0.5	0.5	0.5	0	0.5	0.5
Utilization		100%	100%			100%	100%

6. Battery Life

This section estimates 1998 and 1999 system battery life by looking at factors that affect battery life and projecting typical system power consumption and battery capacity. It also includes suggestions for improving battery life.

6.1 Battery Life Factors and Assumptions

Battery life is affected by many factors including battery capacity, chemistry, discharge rate, discharge profile, temperature and charge/discharge history. These factors are briefly described and some assumptions made to enable a first order battery life estimate for the system described in this paper.

Battery capacity is the total amount of power a battery can deliver when discharged at constant current over a 5 hour period. While there are many different battery sizes in use today, 3x4 cell lithium ion battery stacks are common in many high end systems and will be used for this battery life analysis. A typical 3x4 cell lithium ion battery stack today has roughly 38 watt hours capacity. Assuming approximately 8% per year improvement in capacity due to battery chemistry improvements, typical battery packs in 1998 and 1999 are likely to have a nominal capacities around 41 and 44 watt hours respectively.

Discharge rate has a non-linear impact on the total amount of power a battery can deliver. A battery will deliver its full rated capacity when discharged at constant current over a 5 hour period (called a 1C discharge rate.) If a battery is discharged twice as fast (2C discharge rate) it will not deliver as much total power as it would if discharged at a 1C rate. Table 6.1 shows approximate capacity derating at various discharge rates for lithium ion batteries.

Table 6.1 Battery Capacity at Various Discharge Rates

Discharge Rate	Usable Battery Capacity (Normalized to 1C Discharge Rate)
C/5	107%
C/2	104%
1C	100%
2C	94%
4C	86%

This table is for constant current discharging. Note that discharging faster than a 1C rate decreases usable capacity more than slowing the discharge rate increases capacity. If the discharge rate is not constant, the usable battery capacity will be less than the capacity at the average rate of discharge. For example, if a battery was discharged at a pulsed rate of 2C 50% of the time and C/2 50% the average discharge rate would be 1C but the usable battery capacity would be only 99%.

Usage profile refers to the dynamically changing discharge rates a battery is subjected to during use. The usage profile will vary significantly across users and systems. To measure battery life across various systems a consistent user profile must be established. This guideline uses the SYSMark32 for Battery Life (SYSMark32/BL) benchmark from BAPCO as a consistent user profile. This benchmark approximates a real usage scenario by running scripts for seven applications and entering data at a typing rate of approximately 48 words per minute. The applications include a spreadsheet, database, presentation, personal information manager, a game and two word processing programs. It also includes a 20 minute idle time after completing a loop through all seven applications since typical systems go into standby occasionally.

Battery chemistry affects peak discharge rate, thermal response, and the number of charge / discharge cycles a battery can tolerate. These all impact the useful charge a battery can deliver. Nickel Cadmium (NiCd) and Nickel Metal Hydride (NiMH) have higher peak current capabilities than Lithium ion (Li^+) chemistries but are also more sensitive to temperature. As temperature rises the internal resistance in NiCd and NiMH increases and reduces peak current capability. At room temperature and above, Li^+ peak current capacity is relatively temperature independent. Battery capacity also diminishes as batteries are repeatedly charged and discharged. This battery life analysis assumes a new, fully charged Li^+ battery pack is used and it is at or above room temperature.

6.2 Total System Power Estimates

To estimate system battery life, average power consumption for the entire system must be estimated. This includes the notebook base, LCD, and any peripherals plugged in that draw power from the notebook. This analysis makes the following configuration and usage assumptions:

- The system configuration is the same as shown in Table 5.1.
- There are no devices connected to the external 1394 or USB ports
- The DVD drive is not used while running the SYSMark32/BL benchmark and is in the sleep state.
- The 1394 controller (1999 configuration) is in the suspend state.
- A LAN is connected (CardBus in 1998 and onboard in 1999) and is predominantly idle.
- The power management algorithm puts the hard drive into standby after 2 minutes and to sleep after 5 more minutes.
- The power management algorithm turns off the LCD backlight after 5 minutes of inactivity and suspends after 10 minutes.

Table 6.2 shows the estimated component utilization and power consumption while running the SYSMark32/BL benchmark for both 1998 and 1999 systems. The utilization estimates assume the time required to complete a loop through the SysMark32/BL benchmark is dominated by fixed delays associated with the input typing rate. Higher performance processors will complete tasks faster and spend more time in a low power idle state when waiting for input. Configuration differences and lower component power consumption in 1999 are also factored into the average SysMark32/BL power estimates.

Table 6.2 Estimated SYSMark32 for Battery Life Component Utilization and Power Consumption

	1998		1999	
	Estimated Utilization (%)	Power (Watts)	Estimated Utilization (%)	Power (Watts)
CPU core	33%	3.4	30%	3.0
L2 Cache	Data 20%, Tag 9%	1.0	Data 18%, Tag 8%	0.9
Memory Controller	40%	1.2	40%	0.8
System Memory	40%	1.1	40%	1.2
Graphics Subsystem	40%	2.1	40%	1.7
LCD Panel	86%	2.8	86%	2.0
IO Subsystem	Hub 25%, KBC 75%, ACPI uCtrl 30%	0.5	Hub 25%, KBC 75%, ACPI uCtrl 30%	0.5
Audio	15%	0.6	15%	0.4
Hard Drive	Spin-up 1%, Rd/Wr 20%, Idle 53%, Stdby 15%, Sleep 11%	1.2	Spin-up 1%, Rd/Wr 20%, Idle 53%, Stdby 15%, Sleep 11%	1.2
DVD Drive	0%	0.1	0%	0.1
1394	0%	0.0	0%	0.0
USB	0%	0.0	0%	0.0
Cardbus	5%	1.2	0%	0.1
LAN	0%	0.0	5%	0.4
Power Supply		1.8		1.5
Charging	0%	0.0	0%	0.0
Cooling	10%	0.1	10%	0.1
Other	100%	0.3	100%	0.3
Total SYSMark32/BL System Power		**17.3**		**14.1**

6.3 Battery Life Calculation

With the assumptions and total system power estimates given in the sections 6.1and 6.2 we can calculate the average battery life with the following equation:

Average battery life ≈ ((Battery size * Discharge rate derating) / (Total SYSMark32BL System Power))

Since the estimated total system power is about 42% of the nominal battery capacity in 1998 and 33% in 1999, the batteries will discharge at approximately 2.36 C and 1.66 C rates respectively. Estimating from Table 6.1 these discharge rates will derate the usable battery capacity to approximately 93% of nominal capacity in 1998 and 95% in 1999. This yields the following results:

Average 1998 battery life ≈ ((41 Watt Hours * (0.93)) / (17.3 Watts)) = 2.20 hours

Average 1999 battery life ≈ ((44 Watt Hours * (0.95)) / (14.1 Watts)) = 2.96 hours

These estimates indicate the average battery life for a high end system will be a little more than 2 hours in 1998 and slightly less than 3 hours in 1999. Systems adhering to the mobile power guidelines will benefit from both increased performance and longer battery life since average power is held down while battery capacity is increasing.

6.4 Design considerations

In addition to designing-in lower power components, system vendors can increase battery life by tuning the system and software for lowest power consumption, and implementing aggressive power management strategies.

By using the Intel Power Monitor described in section 4.4, software can be tuned to allow the system to go to lower power states when idle. This tool has been successfully used to identify and correct power wasting code loops in many popular applications and software suites. Using this tool to test future applications can help maximize battery life.

More detailed system tuning can be done with tools such as Intel's Power Analyst (IPA) software. When run with an appropriate hardware setup, the IPA displays subsystem power measurement data in real time. Data for the IPA software comes from a prototype system built with isolated power planes and power measurement sense resistors for each subsystem. The raw power data is collected in a data acquisition module (NetDAQ) and sent to a host computer running the IPA software. The IPA software displays bar graphs simultaneously showing a profile of overall system power and power for each subsystem. This allows system designers to graphically see which subsystems are drawing the most power and to see the correlation in power consumption between all subsystems in real time. The power distribution data can also be used to help identify subsystems that are idle and can be put into lower power states.

System power profiling is an excellent tool for identifying power saving opportunities. Recently, power profiling on an Intel evaluation board helped save almost a watt. Table 6.3 shows the initial CPU power profile during Win'95 idle. This power profile shows the CPU going into the stop clock state between interrupts. It also shows the CPU going to an intermediate power state where the clock is active but the CPU is held inactive for 9 mS before servicing the interrupt. This 9 mS intermediate power state was traced to a bit controlling a timer that set the delay required for CPU clock PLL startup. Since the CPU in this system had a specified clock PLL startup time of 1 mS maximum, reprogramming the bit for 1 mS saved almost 1 watt. Table 6.4 shows the CPU power profile after reprogramming the clock startup timer bit. As future processors come out with lower power states, and lower PLL lock latencies, the power saving opportunities will increase. This example shows the value of system power profiling and identifies attention to correct timer values as an opportunity for improving battery life.

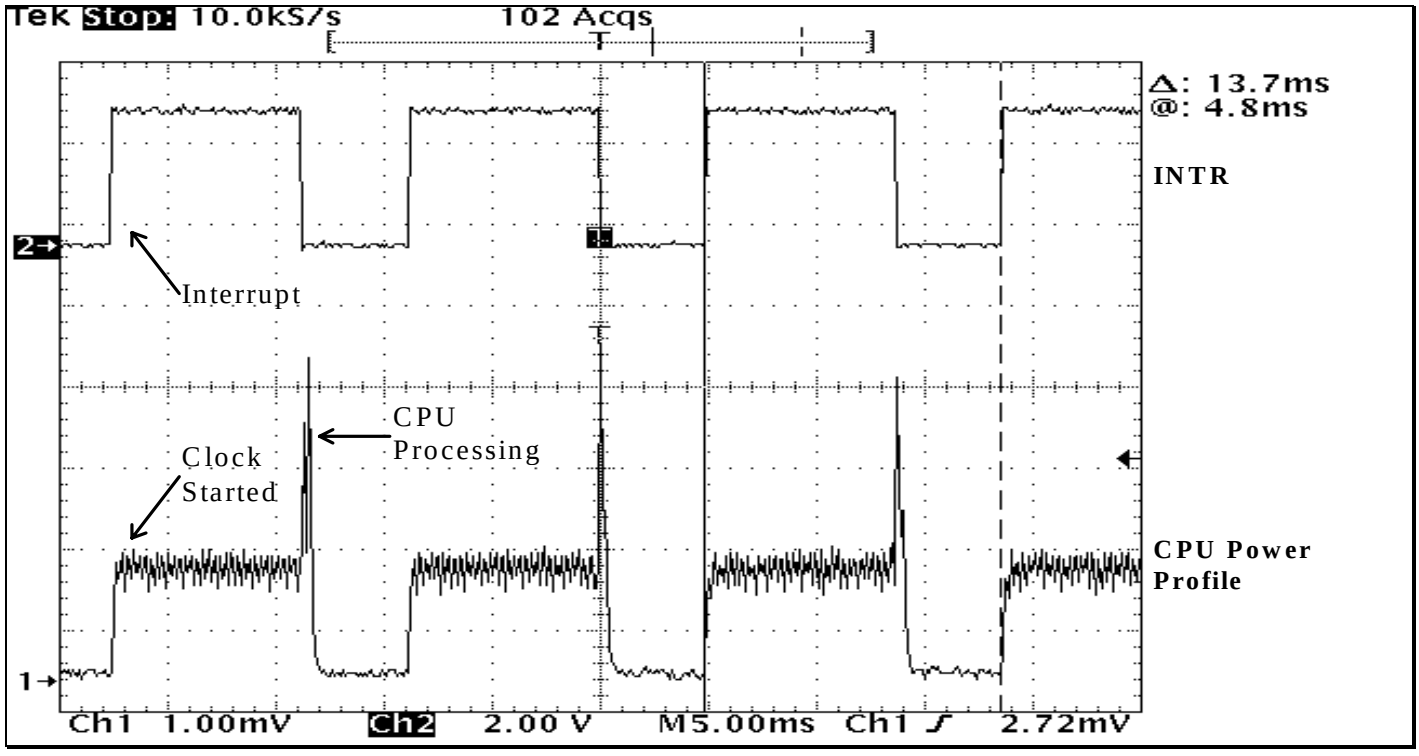

Table 6.3 Initial CPU Power Profile During Win '95 Idle

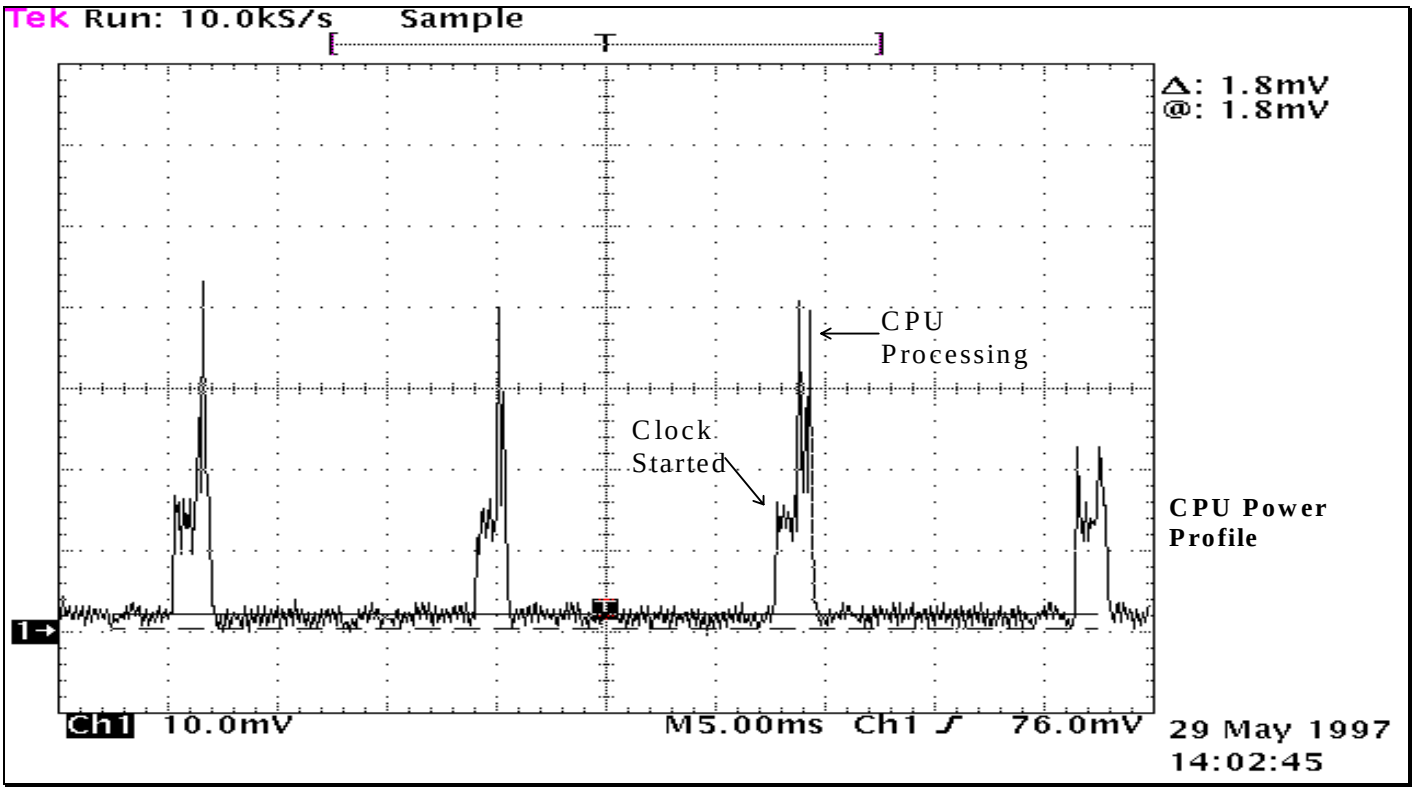

Table 6.4 CPU Power Profile During Win '95 Idle After Timer Optimization

Another way to improve battery life is to implement ACPI power management. This allows the operating system, which has detailed knowledge of what programs are running and what components are being accessed, to put idle components into low power states sooner. This will lower average power consumption and improve battery life.

7. Summary

This paper identifies rising system power consumption and limited thermal dissipation capabilities as barriers to continued notebook computer performance and feature improvements. To address this problem Intel is significantly reducing voltages on mobile system components it manufactures such as the CPU and chip set. Meeting user performance expectations, however, will require moving more components and bus interfaces to lower voltages.

This Mobile Power Guideline suggests component and interface bus voltage and power targets needed to address these system thermal design issues. Component vendors who embrace these power guidelines will benefit from higher performance and lower power products. This will allow them more packaging options and perhaps wider market opportunities. OEM vendors embracing these guidelines will produce higher performance systems with more features and reduced cooling costs. To realize these benefits to the whole industry, we call upon industry leaders like yourselves to join us in bringing about the changes needed to unlock these opportunities on the mobile horizon.

Appendix A. Application Power Consumption

Figure A.1 shows power consumed by several different applications on the same system. This data identified MPEG2 movie playback as the worst case power application we tested in 1997. Extrapolating the subsystem power to 1998 and 1999 and factoring in MPEG algorithm improvements, 3D games are expected to be the worst case power applications in 1998 and 1999.

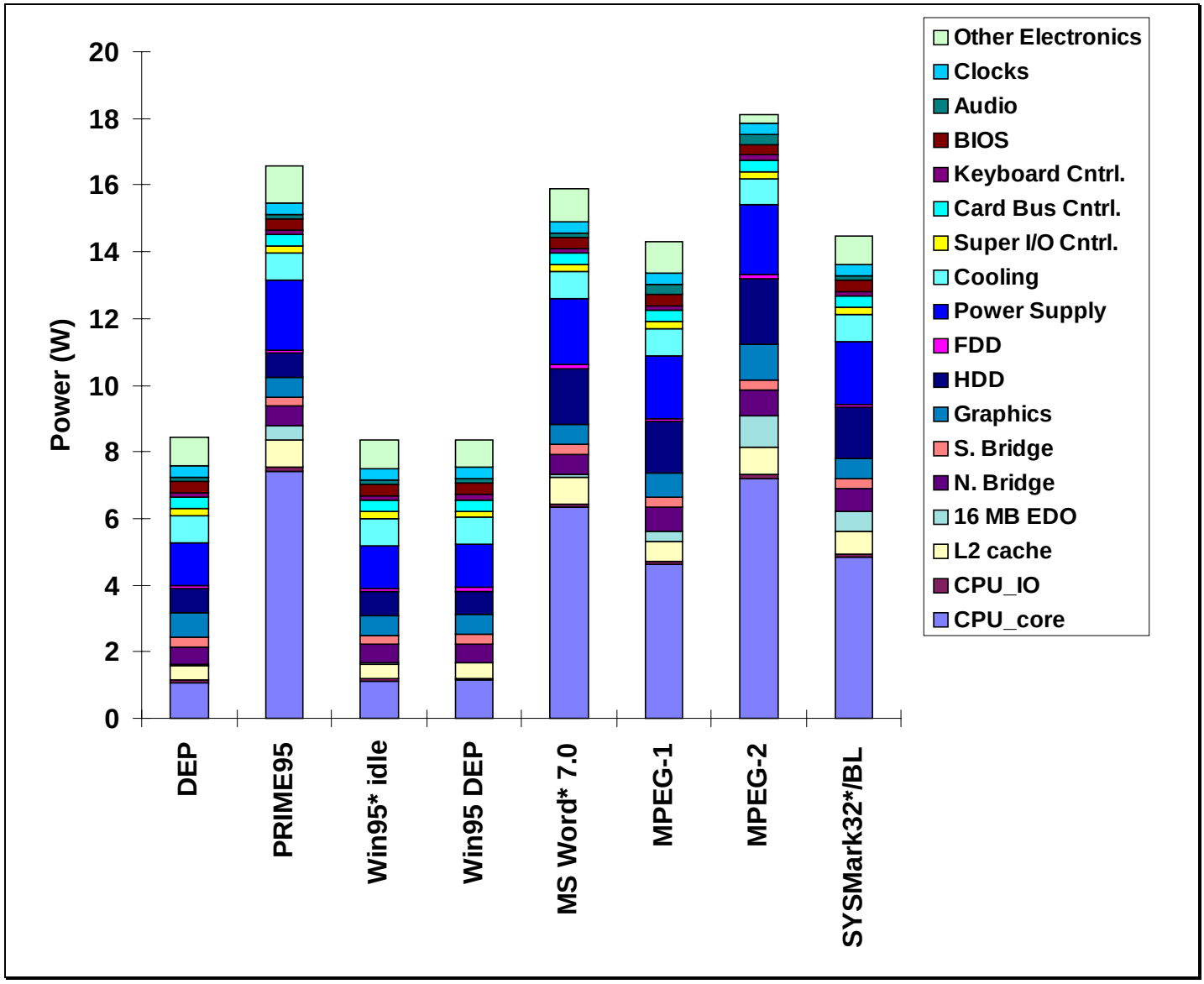

Figure A.1 Power Consumption by Application

The power measurements shown in Figure A.1 were measured on a 166Mhz Pentium Processor with MMX™ technology based platform with 16MB EDO memory and 256KB pipelined burst level two cache. This data includes all components in the notebook interior and excludes LCD panel power. APM power management was enabled during power measurement.

Appendix B. Unmanaged Power Consumption Trend Data and Assumptions

Table B.1 shows the system configurations and worst case applications assumed for the power trend chart shown in **Error! Reference source not found.** and supporting data shown in Table B.2.

Table B.1 Unmanaged Power Trend Configuration Assumptions

	1994	1995	1996	1997	1998	1999
CPU	486 DX4 - 75Mhz	Pentium Processor - 75 Mhz	Pentium Processor - 150 Mhz	Pentium Processor with MMX™ technology - 166 Mhz	Pentium II Processor	Pentium II or next generation Processor
L2 Cache	None	256 KB	256 KB	256 KB	512 KB	512 KB
Memory	8 MB	8 MB FPM	16 MB FPM	16 MB EDO	48 MB SDRAM	48 MB SDRAM (100 Mhz)
Graphics	VL Bus	PCI	PCI	PCI	AGP	AGP-2x
Worst Case Application	DOS* Edit	DOS Edit	DOS Edit	MPEG2 Video	3D Game	3D Game

Table B.2 shows system power trend data in tabular form. Overall system power data for 1994 - 1996 was measured on production systems and the division between subsystems was estimated. 1997 subsystem data was measured on an Intel notebook evaluation platform. 1998 and 1999 data was projected based on data available in January 1997.

Table B.2 Unmanaged Power Consumption Trend Data (in Watts)

	1994	1995	1996	1997	1998	1999
CPU	2.96	6.02	6.61	7.32	8.00	8.60
L2 Cache		0.40	0.75	0.83	1.70	1.80
Memory	0.80	0.60	0.85	0.94	2.00	3.00
Chipset	1.60	1.60	1.80	1.40	4.21	4.95
Graphics	0.70	0.80	0.90	1.05	4.15	6.65
Drives	1.50	1.90	2.04	2.04	3.00	3.50
Power Supply	1.37	1.66	1.96	2.10	3.22	3.50
Super I/O	0.20	0.20	0.20	0.20	0.20	0.20
PCMCIA/Card Bus Controller	0.35	0.35	0.35	0.35	0.35	0.35
Keyboard Controller	0.15	0.15	0.15	0.15	0.15	0.15
Clocks	0.20	0.30	0.30	0.35	0.30	0.30
Audio				0.30	3.00	3.00
Cooling			0.80	0.80	0.50	0.50
Other Electronics			0.60	0.87	1.29	1.29
Total	**9.83**	**13.98**	**17.31**	**18.70**	**32.07**	**37.79**

Appendix C. ACPI Power State Descriptions

Introduction

ACPI is an industry specification drafted by Microsoft, Intel, and Toshiba that specifies a register-level interface to core power management functions and a descriptive interface for additional hardware features. This gives system designers the ability to implement a range of power management features with different hardware designs while using the same operating system driver. ACPI, in addition to enabling operating system-directed power management, provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI leverages the Plug and Play BIOS data structures while providing a processor architecture-independent implementation that is compatible with both Windows 95* and Windows NT*.

This section provides a brief overview of ACPI, adopted from a description found at

http://www.microsoft.com/hwdev/pcfuture/DEVICEPM.HTM

The complete ACPI specification may be found at:

http://www.teleport.com/~acpi/

System Power States

G0, G0/S0

A computer state where the system dispatches user mode (application) threads and they execute. In this state, devices (peripherals) are dynamically having their power state changed.

G1

A computer state where the computer consumes a small amount of power, user mode threads are *not* being executed, and the system "appears" to be off (from an end user's perspective, the display is off, etc.). Latency for returning to the Working state varies on the wakeup environment selected prior to entry of this state (for example, should the system answer phone calls, etc.). Work can be resumed without rebooting the OS because large elements of system context are saved by the hardware and the rest by system software. It is not safe to disassemble the machine in this state. Within this state the system may be in several different sleep states which balance wake up latency against power consumed. S1 is highest in power but lowest in latency. S4 is lowest in power but requires re-load of system context from disk.

Device Power States

Until now, the only description of device power states has been in the APM specification. Unfortunately, these definitions are not precise and have led to a wide variety of interpretations, which has caused problems. To standardize the nomenclature, the definitions presented in this section are used for the power states of devices on any bus. These states are defined in terms of the following four criteria:

Power consumption: how much power the device uses.
Device context: how much of the operational context of the device is retained
Device driver: what the driver does to restore the device to fully on from a given state.
Restore time: how long it takes to restore the device to be fully on.

D3 State for Device Power

Power consumption: Power may be fully removed from the device.
Device state: Device context is lost. As such, it is assumed the state cannot be restored automatically to its prior conditions. The device must be reinitialized to its power-on defaults upon entering a higher power state.
Device drivers: Any device driver associated with the device must reinitialize the device from its power-on defaults when exiting the D3 state for a higher power state.
Restore time: Total restore time for the device is highest because of the need to completely reinitialize the device.

D2 State for Device Power

Power consumption: Power consumption is equal to or greater than the D3 state. Power usage should be reduced to the minimum level where device state restoration is still possible.
Device context: Device context might be preserved or might be lost, depending on class-specific definitions
Device drivers: Device driver function in this state is according to class-specific definitions.
Restore time: The time required to restore the device from the D2 state to the D0 state is equal to or slower than resumption from the D1 state. It is acceptable for device restoration time from D2 to be slower than D1 in the interests of additional power conservation. Actual response times are according to class-specific definitions.

D1 State for Device Power

Power consumption: Power consumption is equal to or greater than the D2 state, but less than the D0 state.
Device context: Device context might be preserved or might be lost, depending on class-specific definitions.
Device drivers: Device driver function in this state is according to class-specific definitions.
Restore time: The time required to restore the device from the D1 state to the D0 state is quicker than resumption from D2 whenever possible. Resumption should incur the least possible delay to avoid user perception of delay. Minimizing delay in restoring the device is a higher priority than power consumption in this state. Actual response times are according to class-specific definitions.

D0 State for Device Power

Power consumption: This is assumed to be the highest level of power consumption.
Device context: The device is completely active and responsive.
Device drivers: The driver is functioning normally.
Restore time: Not applicable.

Self Power Management within a Device State

Devices may have additional “Self Power Management” within a device state provided that external characteristics visible to the operating system such as restore time or latency are not altered. An example of this would be a graphics controller which can remove clocks to internal units when idle but automatically restores clocks within one access cycle when addressed by the CPU.